THEORY & OBJECTIVE

BASIC ELECTRONICS

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SEMICONDUCTOR DIODES

THEORY

1.1 Semiconductor Physics

1.1.1 Energy Bands

In gaseous substances, the arrangement of molecules is not close. In liquids, the molecular arrangement is moderate. But, in solids, the molecules are so closely arranged, that the electrons in the atoms of molecules tend to move into the orbitals of neighbouring atoms. Hence the electron orbital's overlap when the atoms come together.

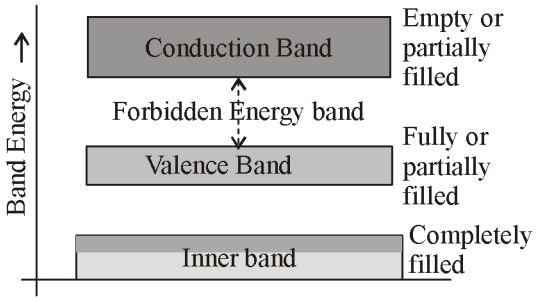
Due to the intermixing of atoms in solids, instead of single energy levels, there will be bands of energy levels formed. These set of energy levels, which are closely packed are called as Energy bands.

(i) Valance Band: The electrons move in the atoms in certain energy levels but the energy of the electrons in the innermost shell is higher than the outermost shell electrons. The electrons that are present in the outermost shell are called as valance electrons. These valance electrons, containing a series of energy levels, form an energy band which is called as valence band. The valence band is the band having the highest occupied energy.

(ii) Conduction Band: The valence electrons are so loosely attached to the nucleus that even at room temperature; few of the valence electrons leave the band to be free. These are called as free electrons as they tend to move towards the neighbouring atoms. These free electrons are the ones which conduct the current in a conductor and hence called as conduction electrons. The band which contains conduction electrons is called as conduction band. The conduction band is the band having the lowest occupied energy.

(iii) Forbidden gap: The gap between valence band and conduction band is called as forbidden energy gap. As the name implies, this band is the forbidden one without energy. Hence no electron stays in this band. The valence electrons, while going to the conduction band, pass through this.

The following figure shows the valance band, conduction band, and the forbidden gap.

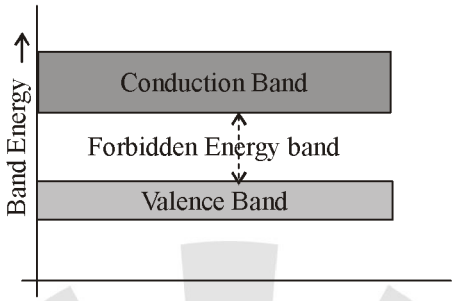


Depending upon the size of the forbidden gap, the Insulators, the Semiconductors and the Conductors are formed.

(a) Insulators: Insulators are such materials in which the conduction cannot take place, due to the large forbidden gap.

Ex. : Wood, Rubber.

The structure of energy bands in Insulators is as shown in the following figure.



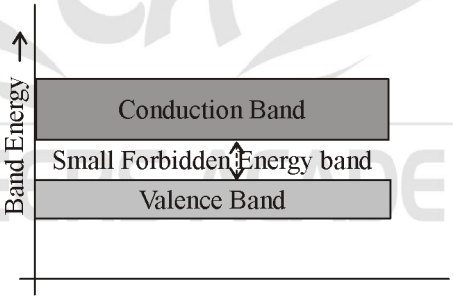
Characteristics: The following are the characteristics of Insulators.

- The Forbidden energy gap is very large.
- Valance band electrons are bound tightly to atoms.
- The value of forbidden energy gap for an insulator will be of 6 eV.
- For some insulators, as the temperature increases, they might show some conduction.
- The resistivity of an insulator will be in the order of 10^7 ohmmeter.

(b) Semiconductors: Semiconductors are such materials in which the forbidden energy gap is small and the conduction takes place if some external energy is applied.

Ex. : Silicon, Germanium.

The following figure shows the structure of energy bands in semiconductors.



Characteristics: The following are the characteristics of Semiconductors.

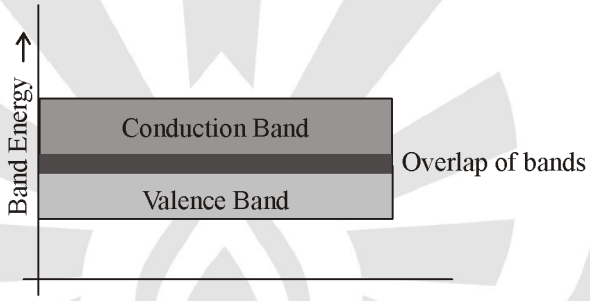
- The Forbidden energy gap is very small.
- The forbidden gap for Ge is 0.7eV whereas for Si is 1.1 eV.
- A Semiconductor actually is neither an insulator, nor a good conductor.
- As the temperature increases, the conductivity of a semiconductor increases.
- The conductivity of a semiconductor will be in the order of 10^2 mhometer.

Semiconductor	Band Gap (eV)
Silicon (Si)	1.1
Germanium (Ge)	0.66
Germanium Arsenide (GaAs)	1.41
Indium Phosphate (InP)	1.34
Zinc tellurite (Zn Te)	2.26
Cudmium Tellurite (CdTe)	1.43

(c) Conductors : Conductors are such materials in which the forbidden energy gap disappears as the valence band and conduction band become very close that they overlap.

Ex. : Copper, Aluminium.

The following figure shows the structure of energy bands in conductors.



Characteristics : The following are the characteristics of Conductors.

- There exists no forbidden gap in a conductor.
- The valance band and the conduction band gets overlapped.
- The free electrons available for conduction are plenty.
- A slight increase in voltage, increases the conduction.
- There is no concept of hole formation, as a continuous flow of electrons contribute the current.

1.1.2 Fermi Level

Fermi energy is expressed in eV. Fermi energy is defined as the maximum energy possessed by an electron at 0 K.

Fermi energy is defined as the maximum kinetic energy possessed by an electron at 0 K.

$$\text{Max. KE} = \frac{1}{2}mV_{max}^2$$

$$E_F = \frac{1}{2}mV_{max}^2$$

$$\text{Max. velocity of } e^- = V_{max} = \sqrt{\frac{2E_F}{m}} \text{ m/sec}$$

Fermi energy is also defined as the energy possessed by fastest moving e^- electron at 0 K.

BIPOLAR JUNCTION TRANSISTOR

THEORY

2.1 INTRODUCTION

A BJT is abbreviated as bipolar Junction Transistor. The term bipolar reflects the fact that both electrons and holes participate in the injection process into the oppositely polarized material.

A transistor is a three layer semiconductor device consisting of either two N and one P layer of material or two P and one N type layer of material, the former is called an NPN transistor while the later is called PNP transistor. A transistor is similar to two diodes connected back to back.

Applications :

Presently the transistors are used in :

(i) High speed computers

(ii) Vehicles

(iii) Satellites

(iv) Communication systems

(v) Power systems

(vi) Switching

2.2 CONSTRUCTION

Transistor has basically three section of doped semiconductor. These sections are known as emitter, base and collector.

(i) Emitter : It is a region on one side of transistor which supplies the charge carriers (electrons or holes) to the other region. The emitter is always forward biased w.r.t. base, so that it can supply a larger number of majority carriers. The width of emitter is moderate i.e. wider than base but smaller than collector. It is heavily doped among the three regions.

(ii) Base : It is middle region that forms two junctions. The base emitter junction is forward biased allowing low resistance for the emitter circuit. The base collector junction is reverse biased and provides high resistance to the collector circuit. It is the thinnest layer and is most lightly doped among the three regions.

(iii) Collector : It is a region situated in the other side of transistor which collects charge carriers. Collector junction is always reverse biased. Its function is to remove charges from its junction with the base. Collector is larger than both emitter and base. Doping of collector is less than doping of emitter but higher than doping of base.

Following points about the transistor should be noted :

- A transistor has a very important property that it can raise the strength of a weak signal, which is called amplification.

- The forward bias voltage V_{EB} is very small where as the reverse voltage V_{CB} is very large.
- The resistance of emitter junction is very small, where as the resistance of collector junction is very large.
- Electrons are majority carriers in N-type and holes are majority carriers in P-type.
- Silicon transistors are used most widely because of their higher voltage rating, greater current rating and less temperature sensitivity.
- In reverse bias, a little amount of current would flow in collector circuit. This is only due to minority carriers and is called collector cut-off current I_{CO} or collector base current when emitter open (I_{CBO}).

2.3 Transistor Biasing

An unbiased transistor is never used in actual practice. Biasing is the process in which transistor terminals are connected to the DC voltage source for proper transistor action. Proper DC biasing prepare the transistor to work in different modes as given in the following table :

S.No.	Mode	Emitter-base junction	Collector-base junction	Remark
1.	**Forward active**	Forward bias	Reverse bias	Amplification mode
2.	**Forward saturation**	Forward bias	Forward bias	Switch ON mode $V_{BE} > V_{CB}$
3.	**Cut-off**	Reverse bias	Reverse bias	Switch OFF mode
4.	**Reverse active or inverted mode**	Reverse bias	Forward bias	Generally not used
5.	**Reverse saturation**	Forward bias	Forward bias	Switch with long turn OFF time and $V_{BE} < V_{CB}$

2.4 Different Operating Conditions of a Transistor

(i) Active Mode : In this mode emitter junction is forward biased and collector junction is reverse biased. Here collector current depends upon the emitter current. Generally transistor is operated in this region for amplification.

(ii) Saturation Mode : In this mode both emitter junction and collector junction are forward biased. Here the collector current is independent of base current. The transistor acts like a closed switch.

(iii) Cut-off Mode : In this mode both emitter junction and collector junction are reverse biased. Emitter does not emit carriers into the base and no carriers are collected by the collector. Thus, transistor acts like an open switch.

(iv) Inverted Mode : In this mode, emitter junction is reverse biased and collector junction is forward biased.

Note : The mode of operation are same for both NPN and PNP transistor. However, in PNP transistor biasing the polarity voltage are opposite to that of NPN transistor.

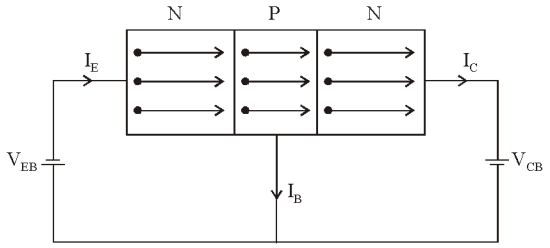
General NPN Transistor Junction Voltages at Room Temperature

	$V_{CE,sat}$	$V_{BE,sat} = V_{\sigma}$	$V_{BE,\ active}$	$V_{BE,cutin} = V_{\gamma}$	$V_{BE,\ cutoff}$
Si	0.2	0.8	0.7	0.5	0.0
Ge	0.1	0.3	0.2	0.1	-0.1

Note : For PNP transistor sign of all the voltages in the above table will be opposite.

2.5 Working of NPN Transistor

Figure below shows an NPN transistor in which emitter-base junction is forward biased and base-collector junction is reverse biased.



The forward bias causes the electrons in N-type emitter to flow towards the base and constitutes the emitter current I_E. In the P-type base, these electrons, combines with the holes. Since base region is thin and lightly doped, only few electrons (less than 5%) combine with the holes to constitute base current I_B. The remaining (more than 95%) moves towards the collector region to constitute the collector current I_C. Therefore, all the emitter current flows towards the collector region. Thus, emitter current is the sum of base and collector current.

i.e. $$I_E = I_C + I_B$$

2.6 Transistor Configuration

A transistor has three terminals namely, emitter, base and collector. When it is used in a circuit, four terminals are needed, two for input and two for output. This problem is solved by making one terminal of the transistor common to both input and output. Therefore, transistor configurations are possible. These are :

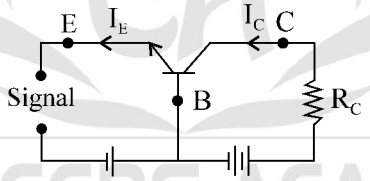
(i) Common Base

(ii) Common Emitter

(iii) Common Collector

2.6.1 *Common Base* :

In common base configuration, input is applied between emitter and base and output is measured between collector and base. Hence base terminal is common for both output and input terminals. Figure given below shows a common base NPN transistor :



Current gain or Current amplification factor is the ratio of output current I_C to input current I_E

i.e. $$\alpha \cong \frac{I_C}{I_E}$$ (assuming zero leakage current from collector junction)

Note: Value of α is less than unity. Practical value of α lies in the range from 0.9 to 0.99.

(i) Input Characteristics :

- The emitter current increases rapidly with a small change in emitter-base voltage. Here input resistance is very small.
- The emitter current is almost independent of collector-base voltage. Input resistance is given by

$$r_i = \frac{V_{EB}}{I_E} \text{ (at constant } V_{CB})$$

FIELD EFFECT TRANSISTORS

THEORY

3.1 INTRODUCTION

FET is a semiconductor device which depends on the control current by an electric field for its operation. Field effect transistor is field controlled device. It is also a three terminal device similar to BJT.

Difference between BJT and FET

	FET		BJT
1.	Voltage controlled current source.	1.	Current controlled current source.
2.	Unipolar device.	2.	Bipolar device.
3.	It require less construction area.	3.	Relatively larger area is required.
4.	High input resistance.	4.	Low input impedance.
5.	There is no offset voltage.	5.	It suffers from offset voltage problem.
6.	Early effect or thermal runaway problem is not observed.	6.	Early effect and thermal runaway problem is observed.
7.	Less noisy.	7.	More noisy.
8.	Gain bandwidth product is small.	8.	Gain bandwidth product is more than FET.
9.	Less sensitive to changes in input signal.	9.	Highly sensitive to changes in input signal.
10.	FET's are more temperature stable than BJTs.	10.	Less temperature stable than FETs.
11	Low power rating.	11	High power rating.

3.2 TYPES OF FET

In field Effect Transistor the output characteristics are controlled by input voltage not by input current as in BJT. There are two basic types of Field Effect transistors, the Junction Field Effect Transistors (JFET) and Metal Oxide Semiconductor Field Effect Transistors (MOSFET).

3.2.1 Junction Field Effect Transistor

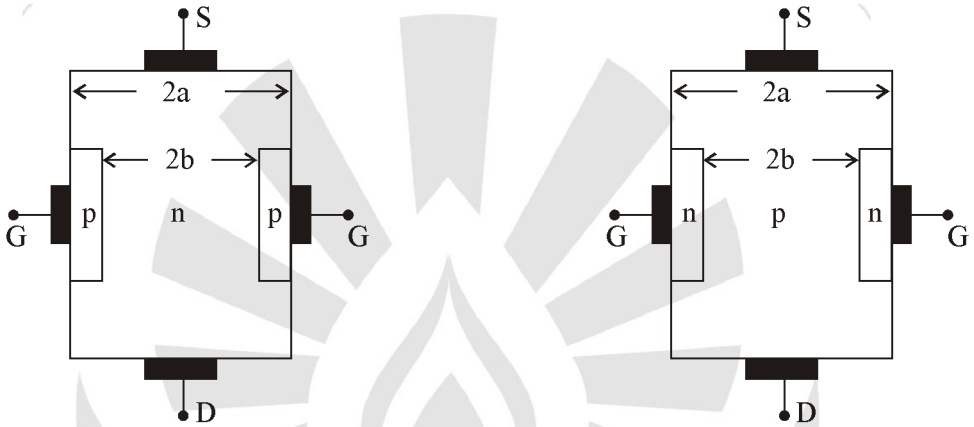
A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e. electrons or holes. JFET are of two types n-channel and p-channel respectively.

The structure of an n-channel and p-channel FET is shown in figure below. A JFET consists of a P-type or N-type silicon bar which contains two pn junctions at the sides. The bar forms the conducting channel for the charge carriers. When bar is of n type it is called n-channel JFET and when it is of P-type it is called p-channel JFET. Two terminal source (S) and drain (D) taken out from bar. They are defined as below :

(i) **Source :** Source (S) is the terminal through which the majority carriers enters the bar and constitutes the source current. This current is designated as I_S.

(ii) **Drain :** Drain (D) is the terminal through which majority carriers leave the bar and constitutes drain current. This current is designated by I_D. The drain to source voltage V_{DS}, drain terminal is more positive than source terminal for n-channel FET (for p-channel V_{DS} is negative).

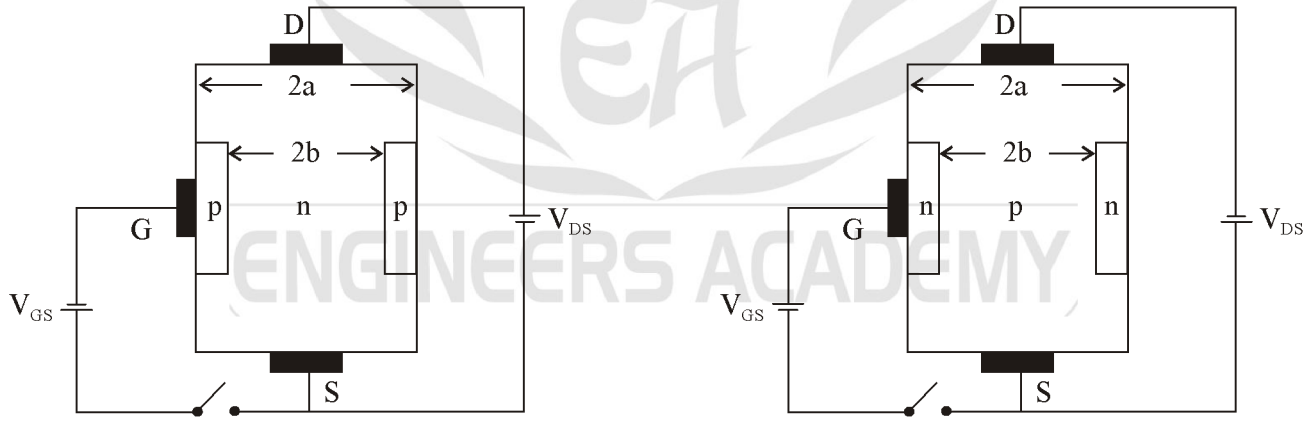
(iii) **Gate :** On both sides of the N-type bar in n-channel JFET, heavily doped p-regions due to acceptor impurities are present. These regions are called Gate (G). The p-n junction between the Gate terminal and source terminal is kept reverse biased. The current in gate terminal is designated as I_G.



n-channel FET p-channel FET

In n-channel conduction is because of flow of electrons, whereas in p-channel conduction is because of holes.

FET Operation : Figure below shows the biasing arrangement for an n-channel JFET and a p-channel JFET. The gate-source terminals are always reverse biased. The drain and source terminals are interchangeable.



In an n-channel JFET, when the voltage V_{DS} is applied between drain and source and V_{GS} is assumed zero. The two pn junctions at the side of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these depletion layers governs the width of the channel and hence the current flowing through the channel.

When a reverse voltage V_{GS} is applied between gate and source. The width of the channel increases as a result of which current through the channel decreases. It means, when reverse voltage V_{GS} increases, the resistance of the n region increases.

Similarly, when reverse gate voltage is decreased, the channel width also decreases and hence current through the channel will be increased.

Shockley Equation : As in BJT, the linear relationship does not exist between the output and the input quantities of a JFET. The relation between I_D and V_{GS} is defined by Shockley's equation given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad ...(i)$$

where $I_D = I_S$

Important terms :

1. **Shorted gate drain current, I_{DSS} :** I_{DSS} is the drain current with source short circuited to gate i.e. $V_{GS} = 0$ and drain voltage equals to pinch off voltage. It is also called zero bias current.

   I_{DSS} is the maximum drain current obtained for normal operation of JFET. Also there is maximum drain voltage V_{DSmax} above which JFET will breakdown.

2. **Pinch OFF voltage, V_P :** It is the maximum drain-source voltage at which the drain current becomes constant. From equation (i), pinch off voltage is defined when $V_{GS} = V_P$ and $I_D = 0$

   For n-channel FET,

$$|V_P| = \frac{qN_D a^2}{2\varepsilon}$$

and $$V_{GS} = \left(1 - \frac{b}{a}\right)^2 V_P$$

where 2a = width of barrier

2b = effective width of channel

3.2.2 Metal Oxide Semiconductor Field Transistor

Metal Oxide Semiconductor Field Transistor (MOSFET) are insulated gate FETs, they don't have any flow of charge carrier through gate region because the gate terminal is insulated from channel or substrate by using SiO_2 layer in between. The input impedance of MOSFET is much greater than JFETs because of very small gate leakage current.

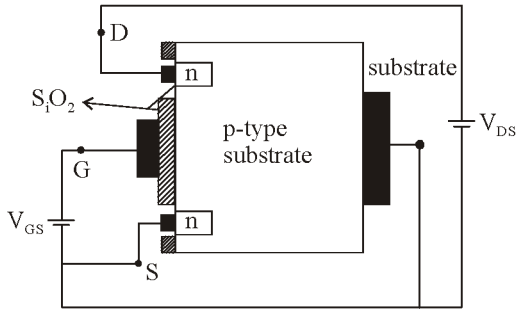
MOSFETs may further be broken into two types :

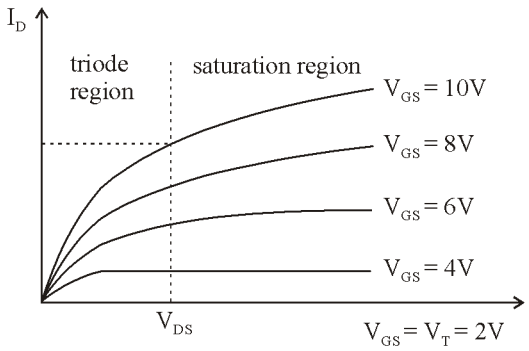
(i) Enhanced type MOSFET

(ii) Depletion type MOSFET

(i) Enhanced type MOSFET : Figure below shows the constructional details of n-channel enhancement type MOSFET. It is similar to JFET except the following :

- Like JFET, a MOSFET has three terminals, source, drain and gate.
- In n-channel MOSFET, two highly doped n-regions are diffused over a P-type substrate. These two n-regions acts as a drain and source. Then metal contacts are connected to drain and source.
- A thin layer of metal oxide is deposited over the left side of the channel. A metallic gate is deposited over the oxide layer. Silicon dioxide (metal oxide) layer is an insulator hence gate is insulated from the channel. Therefore, it is sometimes called Insulated Gate FET.



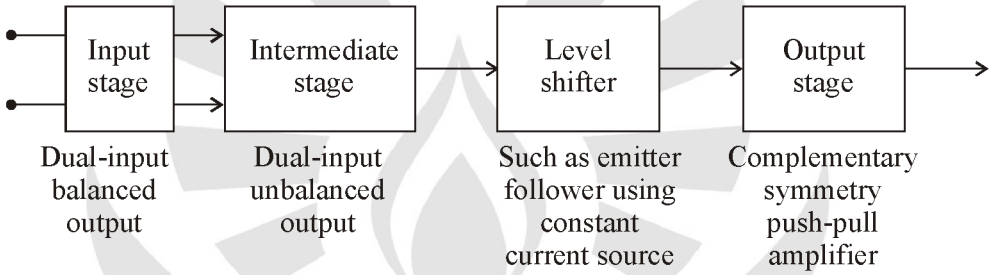


MISCELLANEOUS

THEORY

4.1 Operational Amplifier

The basis of an Op-Amp is a differential amplifier is basically a direct coupled amplifier. Its block diagram is shown below:



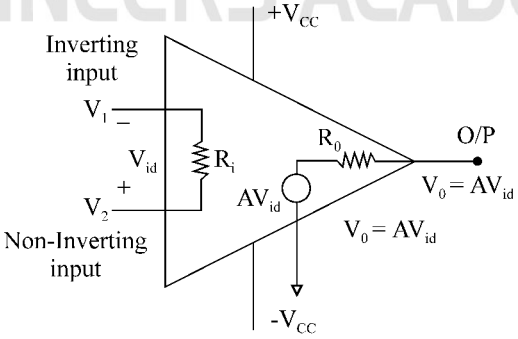
Input Stage : In provides almost all the voltage gain of Op-Amp and also establish the input impedance of Op-Amp.

Intermediate Stage : It provides remaining gain of Op-Amp.

Level Shifting : Because of the direct coupling DC voltage at output is well above the ground level in order to get back the DC level to ground potential. So that variation in output is only because of input signal we use level shifting.

Output stage : It raises the current supplying capability and increases the output voltage swing and this stages proper design will provides the low output resistance.

Equivalent Circuit of an Op-Amp

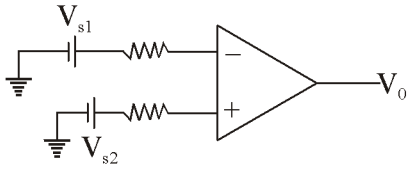


$$V_0 = A(V_1 - V_2) = AV_d$$

4.1.1 Important Terms

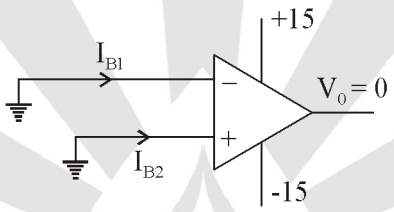
Output Offset Voltage : Output voltage when both the input are grounded is called output offset voltage. It should be zero for ideal voltage.

Input Offset Voltage : The differential input voltage applied at input side to make the output offset voltage zero is called input offset voltage.



$$V_{io} = V_{s1} - V_{s2}$$

Input Offset Current : Algebraic difference between the current of non-inverting and inverting terminals is known as input offset current provided output voltage is zero.



$$I_{i0} = | I_{B1} - I_{B2} |$$

Input Bias Current : Average of two current that flow through inverting and non-inverting terminal is known as input bias current provided output voltage is zero.

$$I_B = \frac{I_{B1} + I_{B2}}{2} \quad \ldots(i)$$

Power Supply Rejection Ratio : Change in input offset voltage with power supply variation is called power supply rejection ratio.

$$PSRR = \frac{\Delta V_{i0}}{\Delta V_{ii}} \quad \ldots(ii)$$

Common Mode Rejection Ratio (CMRR) : It is the most important characteristic of Op-Amp. It is defined as the ratio of differential gain to common mode gain.

$$CMRR = \frac{A_d}{A_{CM}} \quad \ldots(iii)$$

It represents the ability of Op-Amp to reject the common mode signal.

For practical Op-Amp output voltage is given by

$$V_0 = A_d\left(V_d + \frac{V_{CM}}{CMRR}\right) \quad \ldots(iv)$$

where, A_d = differential voltage gain

V_{CM} = common mode input signal

CMRR=common mode rejection ratio

In order to avoid any common mode amplification CMRR should be infinite which can be achieved by increasing R_E because

$$CMRR = \frac{A_d}{A_{CM}}$$

and $$A_{CM} = \frac{R_C}{2R_E}$$

Slew Rate : Maximum rate of change of output voltage w.r.t. time is defined as slew rate :

$$\left|\frac{dV_0}{dt}\right|_{max} = S.R.$$

It represents the how fast output can change with change in the input frequency.

Let output voltage $V_0 = V_m \sin \omega t$

$$\text{Slew Rate} = \left|\frac{dV_0}{dt}\right|_{max} = |V_m \omega|$$

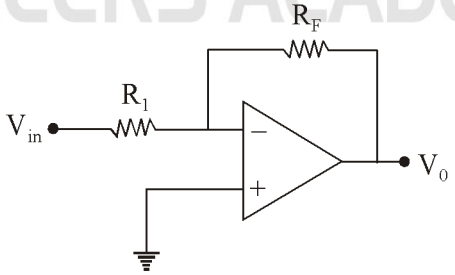
Maximum frequency variation is the sinusoidal output depends on $\frac{S.R.}{V_m 2\pi} = f_{max}$

4.1.2 Properties

Parameters	Ideal values	Practical values
Voltage gain	∞	10^6
Input resistance	∞	$10^6\,\Omega$ or $1\,M\Omega$
Output resistance	0	$10\,\Omega$ to $100\,\Omega$
Bandwidth	∞	10^6 Hz or 1MHz
CMRR	∞	10^6 or 120dB
Slew Rate	∞	$80\,V/\mu sec$

4.1.3 Linear Op-Amp circuits

Inverting Amplifier



It is a voltage shunt configuration

$$A_V = \frac{V_0}{V_{in}} = -\frac{R_F}{R_1}$$

PRACTICE SHEET

OBJECTIVE QUESTIONS

1. The 'slew rate' of an Operational amplifier indicates (when a step input signal is given)
(a) how fast its output current can change
(b) how fast its output impedance can change
(c) how fast its output power can change
(d) how fast its output voltage can change

2. The open loop gain of an Op-Amp available in the market may be around
(a) 10^{-1} (b) 10^{1}
(c) 10^{5} (d) 10^{2}

3. For an Op-Amp having differential gain A_V and common mode gain A_C the CMRR is given by
(a) $A_V + A_C$ (b) $\frac{A_V}{A_C}$
(c) $\left(\frac{A_V}{A_C}\right)+1$ (d) $\frac{A_C}{A_V}$

4. In the common mode is
(a) both inputs are grounded
(b) the outputs are connected together
(c) an identical signal appears on both inputs
(d) the output signals are inphase

5. The common mode gain is
(a) very high (b) very low
(c) always unity (d) unpredictable

6. The differential gain is
(a) very high
(b) very low
(c) dependent on input voltage
(d) about 100

7. If $A_{DM} = 3500$ and $A_{CM} = 0.35$, the CMRR is
(a) 1225 (b) 10,000
(c) 80 dB (d) Both b and c

8. With zero volts on both inputs, an Op-Amp ideally should have an output
(a) equal to the positive supply voltage
(b) equal to the negative supply voltage
(c) equal to zero
(d) equal to the CMRR

9. Of the values listed, the most realistic value for open loop voltage gain of an OP-amp is
(a) 1 (b) 2000
(c) 80 dB (d) 100,000

10. A voltage follower
(a) has a voltage gain of 1
(b) in noninverting
(c) has no feedback resistor
(d) has all of these

11. The common mode voltage gain is
(a) smaller than differential voltage gain
(b) equal to differential voltage gain
(c) greater than differential voltage gain
(d) none of the above

12. The common mode voltage gain of a differential amplifier is equal to RC divided by
(a) r_e' (b) $2r_e'$
(c) $\frac{r_e'}{2}$ (d) $2R_E$

13. Current cannot flow to ground through
(a) a mechanical ground
(b) an AC ground
(c) a virtual ground
(d) an ordinary ground

14. Common mode gain in op-amp
(a) $\frac{R_C}{2R_E}$
(b) $\frac{R_C}{r_e}$
(c) $\frac{R_C}{R_E}$
(d) different for different configurational